ABSTRACT OF THE DISCLOSURE

Quadrature clock generating apparatus includes a multiplexer selecting one of a generated clock and a gated generated clock as a double clock in accordance with a halt multiplexer control. Divider circuitry provides an alignment signal corresponding to an inverted double clock divided by two. A recovery circuit recovers first and second clocks having a 90° phase difference from the double clock in accordance with the alignment signal. A halt circuit controls the halt multiplexer control to select the gated generated clock when the alignment signal matches a pre-determined clock level. The halt multiplexer control is clocked by the generated clock.